Remarks/Arguments:

Claims 1-10 are pending in the application and are rejected. No claims have been amended.

The present invention relates to a digital receiver which includes a signal generator and a baseband transform circuit. Specifically, a frequency divider divides a reference signal and a frequency multiplier multiples the output of the divider by a multiplier value. The output of the frequency multiplier is a product of the output signal of the divider and the multiplier value of the frequency multiplier.

On page 3, the Official Action rejects claims 1-10 under 35 U.S.C. § 103(a) as being unpatentable over Applicants' Admitted Prior Art (AAPA) in view of Takahashi (U.S. Patent No. 5,732,068). It is respectfully submitted, however, that the claims are patentable over the art of record for at least the reasons set forth below.

Applicants' claim 1 is different than Takahashi because Applicants recite a **frequency multiplier** whereas Takahashi teaches a **heterodyning multiplier** that serves as a phase comparator. Applicants frequency multiplier is functionally different than Takahashi's heterodyning multiplier. Specifically, Applicants' frequency multiplier produces a product between an input frequency (multiplicand) and a multiplier value of the frequency multiplier (multiplier). In contrast, Takahashi's heterodyning multiplier produces two sinusoids in which the frequencies are the sum and the difference.

In Fig. 6, Takahashi suggests a heterodyning multiplier 52 that acts as a phase comparator. Specifically, multiplier 52 multiplies the output signal of frequency divider 51 with the output of multiplier 40. These two signals input to multiplier 52 are multiplied together in a mixing procedure which produces a sinusoid having the sum of the two frequencies and another sinusoid having the difference of the two frequencies. By mixing the two inputs, the multiplier 52 is able to compare the phase difference between the inputs. The phase difference between the two signals is then passed through the low pass filter where it controls a variable frequency divider 50. Thus, Takahashi's multiplier, heterodynes (mixes) the output of frequency divider 51 with the output from multiplier 40. This feature is at least supported in Takahashi's

col. 11, line 42 - col. 12, line 25 ("*the output signal of the half frequency divider 51 is applied to multiplier 52. In addition, the output signal of the multiplier 40 which corresponds to the real part is applied to the multiplier 52. The multiplier 52 serves as a phase comparator operating on the output signals of the multiplier 40 and the half frequency divider 51*"). Thus, Takahashi's multiplier 52 is not a frequency multiplier as recited in Applicants' claim 1. Therefore, Applicants respectfully disagree with the Examiner's interpretation of Takahashi.

Applicants' invention, as recited by claim 1, includes a feature which is neither disclosed nor suggested by the art of record, namely:

> **... a frequency multiplier wherein an output frequency of the frequency multiplier is a product of a multiplicand value which is the divided frequency of the first reference signal produced by the frequency divider and a multiplier value of the frequency multiplier ...**

Applicants' claim 1 is different than Takahashi because of a frequency multiplier which produces an output frequency which is the product of the frequency divider output (multiplicand) and a value (multiplier) of the frequency multiplier. For example, assuming the frequency divider output is 1000 Hz and the value of the frequency multiplier is 3, then the output of the frequency multiplier would be the product or 1000 x 3 = 3000 Hz. This frequency multiplier is completely different than the heterodyning multiplier 52 as shown in Fig. 6 of Takahashi. Takahashi's multiplier 52 mixes the two input sinusoids. Therefore, the combination of Takahashi's mixing multiplier 52 with AAPA would not teach the feature of Applicants' claim 1 (Takahashi's mixing multiplier 52 is not a frequency multiplier).

Accordingly, for the reasons set forth above, claim 1 is patentable over the art of record.

Claims 2-10 include all the features of claim 1 from which they depend. Thus, claims 2-10 are also patentable over the art of record for at least the reasons set forth above.

In view of the arguments set forth above, the above identified application is in condition for allowance which action is respectfully requested.

Respectfully submitted,

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Dated: February 26, 2009

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SO_388534